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Obtained after **place** and **route**, final result of the **place** and **route** phase. ...
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erated using the Zippy **place** and **route** tools. Figure 4. shows that for this implementation ... a coarse-grained multi-**context** reconfigurable **array**. A dis- ...
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HLL Program. **Compiler** & Optimizations. (msec to sec). Y. **Place** & **Route**. (minutes to ... In this **context**, resources are defined to be the ...
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[PDF] What Is a **Compiler** When The What Is a **Compiler** When The ...
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Multi-**context**. Reconfigurable Logic. **Array**. **Array** Register File ... **Place** and **route** inherently complex. • Would like to have **compile** times of the order of ...
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[PPT] PowerPoint-Präsentation
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place & **route** tools. fully parameterized to support all Zippy architecture ...
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Transit Note #119 D/FPGAs in an ASIC Core Cell Methodology
Once the **array** is generated, the **compiled array** should, in fact, ... from core or memory blocks to the vendor's backend **placement** and **routing** process. ...
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FPL 2001
Gambit: A Tool for the Simultaneous **Placement** and Detailed **Routing** of Gate-**Arrays**. 243-253 Electronic Edition (link) BibTeX ...
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The **compiler** uses a greedy **place**-. and-**route** algorithm to map these pipe stages onto the ... RC **Array Context**. Configurations. Figure 5: Flow of **Compilation** ...
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EETimes.com
Figure 1 depicts the current FPGA design process **context**: using ... After **placement**, PPR proceeded to **route**. In this design, two time specs were usedone ...
www.eetimes.com/editorial/1996/fpgafeature9601.html - 80k - Cached - Similar pages

[PDF] Dr. José L. Muñoz
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FPGA FPGA. **Compiler**. Mapper. Estimator. C. VHDL/Verilog. **Place**. &. **Route**. Simulation. ACS Program ... ACS RISC + Reconfigurable **Array** architectures entering ...
ehw.jpl.nasa.gov/events/nasa_eh/papers/ACS-EH99-JoseMunoz.pdf - Similar pages

picoChip - picoChip - Frequently Asked Questions
... it doesn't matter: you write the code, **compile** it and **place** in **array**. ...
For FPGAs that provide the same functionality the **place** and **route** time is ...
www.picochip.com/technology/faq - 37k - Cached - Similar pages

Michigan Land Use Institute: Making Smart Growth a Reality In Michigan
New **Route** to Transportation Design Michigan prepares to harmonize highway, ...
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Each **array** element contains its own memory block to store individual configuration bits, where each set of configuration is a ``**context**'' programmed to ...
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To improve throughput and the distribution of design tasks, an intuitive mechanism to **compile** the necessary vendor libraries for post-**place**-and-**route** ...
dataweek.co.za/news.asp?pklNewsId=16201&pklIssueId=524&pklCategoryID=35 - 41k - Cached - Similar pages

Algorithmic and Theoretical Problems Related to the Physical ...
51 The Timberwolf **Placement** and **Routing** Package (**context**) - Sechen, Sangiovanni-Vincentelli - 1985 44 A Detailed Router for Field-Programmable Gate **Arrays** ...
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Wong used **matrix** synthesis problem (MSP) to model the. thermal **placement** problem and three ... decoupled from its physical **PE mapping** in the previous ...
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tima.imag.fr/mpsoc/2004/slides/Wehn.pdf - Similar pages

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are the PADDI-2, the **MATRIX**, and, as reconfigurable coprocessors, the REMARC ... **mapping** and **placement** in one step and a simple greedy **routing** algorithm. ...
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FPGA I/O ports for the whole design can be **mapped** to the device pins using the high-level ... and the **place** and **route** timing netlist is generated. ...
www.xilinx.com/publications/xcellonline/xcell_53/xc_bioinfo53.htm - 38k - Cached - Similar pages

TechOnLine - Reconfigurable Processors: Changing the Systems ...
The first differentiation we experienced with the reconfigurable processor solution over FPGAs solution was the deterministic **place** and **route**. We could **map** ...
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As seen in 2.1, we obtain a 2D **pe** array from the **mapping**. step. Hence two single hyperplanes ... computation time (for **place** and **route**) on a recent work- ...
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> [PDF] Combined Instruction and Loop Parallelism in Array Synthesis for FPGAs
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> moved into the **pe** data-path using standard commerecial. circuit retimers. Our experiments (based on performance es-. timates after **place**-and-**route**) have ...

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matrix. FPGA mapping begins by dividing the circuit. into pieces of sequential logic (logic nodes), ... placement and routing in the hand-mapped. version. ...
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and execute technology mapping, placement, and routing. Such. compilation would be done on a small lean processor coexisting. on the FPGA for this purpose, ...
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the previous switch matrix and attempt to route the wire in the ... technology mapping, and place and route. Code Size is the ...
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Comparison Matrix
LeonardoSpectrum Comparison Matrix. ... Integration w/ FPGA vendor Floorplanning, Place & Route Tools. a. a. ¨ Can assign synthesized cells to physical ...
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fers an integrated FPGA design system with placement hints. at the design entry level. ... technology mapping to place and route. Trianus is currently ...
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